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INTELLECTUAL PROPERTY LAW

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June 5, 2008
March 28, 2008

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Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: **CERTIFICATE OF CORRECTION**
U. S. Letters Patent No. 7,318,115
Issued: January 8, 2008
For: IC MEMORY COMPLEX WITH CONTROLLER
FOR CLUSTERS OF MEMORY BLOCKS I/O
MULTIPLEXED USING COLLAR LOGIC
Inventor: Kanapathippillai et al.
Our File No. 42390.P14037D3

Dear Sir:

Enclosed is the Certificate of Correction for the above-referenced patent.
This request for correction is made under rule 322 of the Rules of Practice and 35 U.S.C.
Section 254.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

EHT
Edwin H. Taylor
Reg. No. 25,129

EHT/dn
Enclosures

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,318,115
DATED : January 8, 2008
INVENTOR(S) : Kanapathippillai et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 17, at line 17, delete "bSP" and insert --DSP--.

MAILING ADDRESS OF SENDER
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PATENT NO. 7,318,115

Certificate of Correction (PTO Form 1050)-Amended